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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,069	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/31/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/31/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending.

2. The office acknowledges the following papers:

Foreign priority papers filed on 3/15/2004,

Drawings filed on 2/2/2004.

Priority

3. This application claims priority to provisional application 60/400,391. The effective filing date for those claims which have proper support in the provisional application is 7/31/2002.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation from claims 6, 13, and 28 "wherein the pre-decode logic is adapted to pre-decode the predetermined prefix concurrently with a preceding instruction" must be shown or the feature(s) canceled from the claim(s). Also, the limitation from claims 14 and 29 "wherein the step of decoding instructions from one instruction set and the step of detecting a predetermined prefix occur sequentially" must be shown or the feature(s) canceled from the claim(s). Also, the limitation from claim 20 "wherein the decoding logic skips decoding of the predetermined prefix and decodes the succeeding instruction immediately following the instruction from the first instruction set" must be

shown or the feature(s) canceled from the claim(s). No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

Specification

5. The disclosure is objected to because of the following informalities:

6. The section titled cross-reference to related applications cites cases related, but leaves out the serial numbers. The serial numbers of the applications should be added, or the patent numbers should be added if applicable.

7. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.

8. Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United

States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

10. Claims 1-4, 7-10, 24-25, and 30 are rejected under 35 U.S.C. §102(e) as being anticipated by McGrath et al. (U.S. 6,560,694).

11. As per claim 1:

McGrath disclosed a processor, comprising:

Decode logic adapted to decode system commands (McGrath: Column 9 lines 26-55)(It's inherent that the processor decodes the SYSCALL instruction so that the correct call to an OS routine can be made.) and instructions in a first mode and in a second mode, wherein the first mode corresponds to a first instruction set and the second mode corresponds to a second instruction set (McGrath: Figures 5 and 6, column 10 lines 20-62)(Figure 6 shows multiple instruction sets accessed through mode bits. One instruction set could be the ISA operating in 16 bits and another instruction set could be the ISA operating in 32 bits.), and wherein the system commands are accessible in either mode through a common Bytecode (McGrath: Column 9 lines 26-55)(A Bytecode is an instruction that can be executed by a processor. A plurality of Bytecodes can comprise an instruction. Either ISA can call an OS routine through a SYSCALL instruction, which is a plurality of Bytecodes in length.).

12. As per claim 2:

McGrath disclosed the processor of claim 1, wherein the system commands belongs to the first instruction set (McGrath: Column 9 lines 26-55)(The SYSCALL instruction can be executed in multiple modes of execution, each of which constitutes a separate ISA.).

13. As per claim 3:

McGrath disclosed the processor of claim 1, wherein the system commands belongs to the second instruction set (McGrath: Column 9 lines 26-55)(The SYSCALL instruction can be executed in multiple modes of execution, each of which constitutes a separate ISA.).

14. As per claim 4:

McGrath disclosed the processor of claim 1, wherein the common Bytecode corresponds to a predetermined prefix, wherein the first and second instruction set each comprises the predetermined prefix (McGrath: Column 9 lines 26-55)(A predetermined prefix is an instruction that indicates at least one system command will follow. The SYSCALL instruction indicates that a system call will be made to execute an OS routine. Thus, it indicates at least one system command will follow.).

15. As per claim 7:

McGrath disclosed the processor of claim 4, wherein the predetermined prefix indicates that a system command follows (McGrath: Column 9 lines 26-55)(A predetermined prefix is an instruction that indicates at least one system command will follow. The SYSCALL instruction indicates that a system call will be made to execute an OS routine. Thus, it indicates at least one system command will follow.).

16. As per claim 8:

The processor of claim 4 wherein the predetermined prefix is decoded (McGrath: Column 9 lines 26-55)(It's inherent that the processor decodes the SYSCALL instruction so that the correct call to an OS routine can be made.).

17. As per claim 9:

McGrath disclosed a method, comprising:

Decoding instructions from one instruction set in a current mode (McGrath: Figure 1 element 14, column 3 lines 46-56; Figures 5 and 6, column 10 lines 20-62)(Figure 1 shows the execution core executing instructions from multiple ISA's. The execution core inherently decodes instruction from multiple ISA's in order to correctly execute them. Figure 6 shows multiple instruction sets accessed through mode bits. One instruction set could be the ISA operating in 16 bits and another instruction set could be the ISA operating in 32 bits.);

Detecting a predetermined prefix indicating a succeeding instruction is a system command (McGrath: Column 9 lines 26-55)(The SYSCALL instruction indicates that a system call will be made to execute an OS routine. Thus, it indicates at least one system command will follow); and

Decoding the system command when executing instruction in the current mode (McGrath: Column 9 lines 26-55)(It's inherent that the processor decodes the SYSCALL instruction so that the correct call to an OS routine can be made.).

18. As per claim 10:

Claim 10 essentially recites the same limitations of claim 5. Therefore, claim 10 is rejected for the same reasons as claim 5.

19. As per claim 24:

McGrath disclosed a system, comprising:

Main processor (McGrath: Figure 12, column 16 lines 41-67 continued to column

17 lines 1-61)(Figure 12 shows many processing elements and one could be considered the main processor and another the co-processor.);

Co-processor coupled to the main processor (McGrath: Figure 12, column 16 lines 41-67 continued to column 17 lines 1-61)(Figure 12 shows many processing elements and one could be considered the main processor and another the co-processor.), the co-processor comprising:

Decode logic adapted to decode instructions from a first instruction set in a first mode and decode instructions from a second instruction set in a second mode (McGrath: Figures 5 and 6, column 10 lines 20-62)(Figure 6 shows multiple instruction sets accessed through mode bits. One instruction set could be the ISA operating in 16 bits and another instruction set could be the ISA operating in 32 bits.); and

Wherein upon detecting a predetermined prefix indicating a succeeding instruction is a system command, stay in the current mode (McGrath: Column 9 lines 26-55)(When a SYSCALL instruction is detected, the mode of execution stays the same. The mode of execution only changes based on other instructions that set a different mode of execution within the instruction bits as shown in figures 2 and 3.).

20. As per claim 25:

Claim 12 essentially recites the same limitations of either claims 2 or 3. Therefore, claim 12 is rejected for the same reasons as either claims 2 or 3.

21. As per claim 30:

The system of claim 24, wherein the system comprises a cellular telephone (Official notice is taken that the processing system could be part of a cellular telephone.).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 5, 11-12, 14-15, 19, 26, and 29 are rejected under 35 U.S.C. §103(a) as being unpatentable over McGrath et al. (U.S. 6,560,694).

24. As per claim 5:

McGrath disclosed the processor of claim 4.

McGrath failed to teach the predetermined prefix is a Java Impdep2 Bytecode.

However, these differences are only found in the nonfunctional descriptive material and are not functionally involved in the steps recited. The system commands are accessible to both instruction set architectures regardless of the predetermined prefix being a Java Impdep2. Thus, this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, *see In re Gulack,* 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); *In re Lowry*, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use any type of predetermined prefix to show the next instruction is a system command because the subjective interpretation of the data does not patentably distinguish the claimed invention.

25. As per claim 11:

Claim 11 essentially recites the same limitations of claim 5. Therefore, claim 11 is rejected for the same reasons as claim 5.

26. As per claim 12:

Claim 12 essentially recites the same limitations of either claims 2 or 3. Therefore, claim 12 is rejected for the same reasons as either claims 2 or 3.

27. As per claim 14:

McGrath disclosed the method of claim 9, wherein the step of decoding instructions from one instruction set and the step of detecting a predetermined prefix occur sequentially (It would have been obvious to one of ordinary skill in the art that the processor without predecode logic would have decoded an instruction from an ISA and detected a SYSCALL instruction sequentially because they are done in the same step at the decoder.).

28. As per claim 15:

Claim 15 essentially recites the same limitations of claim 8. Therefore, claim 15 is rejected for the same reasons as claim 8.

29. As per claim 19:

Claim 19 essentially recites the same limitations of claim 5. Therefore, claim 19 is rejected for the same reasons as claim 5.

30. As per claim 26:

Claim 26 essentially recites the same limitations of claim 5. Therefore, claim 26 is rejected for the same reasons as claim 5.

31. As per claim 29:

Claim 29 essentially recites the same limitations of claim 14. Therefore, claim 29 is rejected for the same reasons as claim 14.

32. Claims 6, 13, 16-18, 20-23, and 27-28 are rejected under 35 U.S.C. §103(a) as being unpatentable over McGrath et al. (U.S. 6,560,694), further in view of Park et al. (U.S. 6,832,305).

33. As per claim 6:

McGrath disclosed the processor of claim 4.

McGrath failed to teach wherein the processor further comprises a pre-decode logic coupled to the decode logic, and wherein the pre-decode logic is adapted to pre-decode the predetermined prefix concurrently with a preceding instruction.

However, Park disclosed wherein the processor further comprises a pre-decode logic coupled to the decode logic, and wherein the pre-decode logic is adapted to pre-decode concurrently with a preceding instruction (Park: Figure 1 element 113 and 170, column 4 lines 1-30).

The advantage of using a predecoder in a multiple ISA system is that the processor will know sooner which type of instruction is being fetched. The decoder will then correctly decode according to the information gathered by the predecoder. One of ordinary skill in the art at the time of the invention would have been motivated by correctly decoding instructions earlier to implement a predecoder. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a predecoder to correctly decode instructions quicker than letting the decoder do both tasks.

McGrath and Park failed to teach wherein the pre-decode logic is adapted to pre-decode the predetermined prefix concurrently with a preceding instruction.

However, it would have been obvious to one of ordinary skill in the art to implement the predecoder to detect the SYSCALL instructions. A SYSCALL instruction is essentially an unconditional branch instruction. By having a predecoder detect SYSCALL instructions, it's possible to fetch instructions needed to execute for the system routine without waiting for the jump address to be fetched after the decoding state. Accordingly, the predecoder will result in increased performance due to the system routine being executed quicker. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the predecoder of Park to predecode for SYSCALL instructions in McGrath for the advantage of executing system routines quicker.

34. As per claim 13:

Claim 13 essentially recites the same limitations of claim 6. Therefore, claim 13 is rejected for the same reasons as claim 6.

35. As per claim 16:

McGrath disclosed a processor, comprising:

Decode logic adapted to decode instructions from a first instruction set in a first mode and decode instructions from a second instruction set in a second mode (McGrath: Figure 1 element 14, column 3 lines 46-56; Figures 5 and 6, column 10 lines 20-62)(Figure 1 shows the execution core executing instructions from multiple ISA's. The execution core inherently decodes instruction from multiple ISA's in order to correctly execute them. Figure 6 shows multiple instruction sets accessed through mode bits. One instruction set could be the ISA operating in 16 bits and another instruction set could be the ISA operating in 32 bits.);

Wherein while the decode logic is decoding an instruction from the first instruction set or a second instruction set, the decode logic detects a predetermined prefix indicating a succeeding instruction is a system command, the decode logic remains in a current mode and decodes the succeeding instruction (McGrath: Column 9 lines 26-55)(When a SYSCALL instruction is detected, the mode of execution stays the same. The mode of execution only changes based on other instructions that set a different mode of execution within the instruction bits as shown in figures 2 and 3.).

McGrath failed to teach pre-decode logic coupled to the decode logic, wherein the pre-decode logic is adapted to pre-decode instructions prior to loading the instruction into the decode logic and wherein the pre-decode logic is adapted to pre-

decode the predetermined prefix concurrently with a preceding instruction.

However, Park disclosed pre-decode logic coupled to the decode logic, wherein the pre-decode logic is adapted to pre-decode instructions prior to loading the instruction into the decode logic (Park: Figure 1 element 113 and 170, column 4 lines 1-30); and

The advantage of using a predecoder in a multiple ISA system is that the processor will know sooner which type of instruction is being fetched. The decoder will then correctly decode according to the information gathered by the predecoder. One of ordinary skill in the art at the time of the invention would have been motivated by correctly decoding instructions earlier to implement a predecoder. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a predecoder to correctly decode instructions quicker than letting the decoder do both tasks.

McGrath and Park failed to teach wherein the pre-decode logic is adapted to pre-decode the predetermined prefix concurrently with a preceding instruction.

However, it would have been obvious to one of ordinary skill in the art to implement the predecoder to detect the SYSCALL instructions. A SYSCALL instruction is essentially an unconditional branch instruction. By having a predecoder detect SYSCALL instructions, it's possible to fetch instructions needed to execute for the system routine without waiting for the jump address to be fetched after the decoding state. Accordingly, the predecoder will result in increased performance due to the system routine being executed quicker. Thus, it would have been obvious to one of

ordinary skill in the art at the time of the invention to implement the predecoder of Park to predecode for SYSCALL instructions in McGrath for the advantage of executing system routines quicker.

36. As per claim 17:

Claim 17 essentially recites the same limitations of claim 16. Therefore, claim 17 is rejected for the same reasons as claim 16.

37. As per claim 18:

Claim 18 essentially recites the same limitations of claim 16. Therefore, claim 18 is rejected for the same reasons as claim 16.

38. As per claim 20:

McGrath and Park disclosed the processor of claim 16, wherein the decode logic skips decoding of the predetermined prefix and decodes the succeeding instruction immediately following the instruction from the first instruction set (McGrath: Column 9 lines 26-55)(The SYSCALL instruction is an unconditional branch instruction. A special register is used to hold the target address for the OS routine that the SYSCALL instruction is calling. The predecode logic is now capable of detecting and jumping to the address of the OS routine to begin fetching instructions to execute. Since the call is an unconditional branch that requires no calculation by the processor to calculate the target address, it would have been obvious to one of ordinary skill in the art at the time of the invention that the SYSCALL instruction could be dropped from execution and that the OS routine could begin executing right away instead of waiting for the SYSCALL instruction to execute.).

39. As per claim 21:

Claim 21 essentially recites the same limitations of claim 8. Therefore, claim 21 is rejected for the same reasons as claim 8.

40. As per claim 22:

Claim 22 essentially recites the same limitations of claim 2. Therefore, claim 22 is rejected for the same reasons as claim 2.

41. As per claim 23:

Claim 23 essentially recites the same limitations of claim 3. Therefore, claim 23 is rejected for the same reasons as claim 3.

42. As per claim 27:

Claim 27 essentially recites the same limitations of claim 6. Therefore, claim 27 is rejected for the same reasons as claim 6.

43. As per claim 28:

Claim 28 essentially recites the same limitations of claim 6. Therefore, claim 28 is rejected for the same reasons as claim 6.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sampsell et al. (U.S. 6,256,714), taught a Java processor with bytecode system calls.

Nguyen et al. (U.S. 6,412,021), taught a Java processor with bytecode system calls.

Barry et al. (U.S. 6,842,811), taught a processor with system calls and multiple modes of execution.

Gorishek, IV et al. (U.S. 6,480,952), taught a processor that can execute multiple instruction set architectures and has instructions to make system calls.

Hammond et al. (U.S. 6,584,558), taught a processor that can execute multiple instruction set architectures and has instructions to make system calls.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183

EDDIE CHAN
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